# EXHIBIT B

**UNITED STATES DISTRICT COURT**
**FOR THE DISTRICT OF MASSACHUSETTS**

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| SINGULAR COMPUTING LLC, | Civil Action No. 1:19-cv-12551 FDS |
| Plaintiff, | |
| v. | Hon. F. Dennis Saylor IV |
| GOOGLE LLC, | |
| Defendant. | |

RESPONSIVE CONTENTIONS REGARDING
NON-INFRINGEMENT AND INVALIDITY

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| U.S. Patent No. 5,442,577 ("Cohen") | August 15, 1995 |
| U.S. Patent App. Publ. No. 2007/0203967 ("Dockser") | August 30, 2007 |
| U.S. Patent Appl. Publ. No. 2009/0066164 ("Flynn") | March 12, 2009 |
| U.S. Patent No. 5,666,071 ("Hawkins") | September 9, 1997 |
| U.S. Patent No. 5,689,677 ("MacMillan") | November 18, 1997 |
| U.S. Patent No. 6,311,282 ("Nelson") | October 30, 2001 |
| U.S. Patent Appl. Pub. No. 2003/0204750 ("Youngs") | October 30, 2003 |

| Prior Art References | Date |
|---|---|
| Adaptive Solutions Connected Network of Adaptive Processors (CNAPS) Neurocomputer Chip ("CNAPS") | 1991 |
| Arnold et. al, "Splash 2" *Proceedings of the 4th Annual ACM Symposium on Parallel Algorithms and Architectures* ("Splash 2") | June 1992 |
| Aty et al, *High-Speed, Area-Efficient FPGA-Based Floating-Point Multiplier* ("Aty") | December 9-11, 2003 |
| Belanović, *Library of Parameterized Hardware Modules for Floating-Point Arithmetic with an Example Application* ("Belanović") | May 2002 |
| Belanović and Leeser, *Library of Parameterized Floating-Point Modules and Their Use* ("Belanović and Leeser") | 2002 |
| Cray T3D System ("Cray T3D") | 1994 |
| Hoefflinger et. al, *Digital Logarithmic CMOS Multiplier for Very-High-Speed Signal Processing* ("Hoefflinger") | 1991 |
| Intel x86 Microprocessor Architecture, including the 80386 microprocessor and 80387 co-processor and the 80486 microprocessor | 1985/1989 |
| Intel i860 Microprocessor Architecture, including the iPSC/860 massively parallel supercomputer system | 1990 |
| Lee et al, *An FPGA-Based Face Detector Using Neural Network and a Scalable Floating Point Unit*, Proceedings of the 5th WSEAS | 2006 |

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| International Conference on Circuits, Systems, Electronics, Control & Signal Processing at 315-320 ("Lee") | |
| Makino, *Grape and Project Milkyway*, Proceedings of the 6th East Asian Meeting of Astronomy | October 18-22, 2004 |
| Makino et al, *GRAPE-6: Massively-Parallel Special-Purpose Computer for Astrophysical Particle Simulation*s, Astronomical Society of Japan | 1993 |
| MANTRA I | 1993 |
| Okumura et al, *GRAPE-3: Highly Parallelized Special-Purpose Computer for Gravitational Many-body Simulations* ("GRAPE-3") | 1992 |
| Okumura et al, *Highly Parallelized Special-Purpose Computer, GRAPE-3*, Astronomical Society of Japan | 1992 |
| Shirazi et al, *Quantitative Analysis of Floating Point Arithmetic on FPGA Based Custom Computing Machines* ("Shirazi") | April 1995 |
| SPERT-II | 1995 |
| Sudha et al, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation* ("Sudha") | 2007 |
| Tong et al, *Reducing Power by Optimizing the Necessary Precision/Range of Floating-Point Arithmetic* ("Tong") | June 2000 |
| SYNAPSE-1 | 1993 |
| Texas Instruments TMS320C32 DSP | 1995 |
| Xilinx Virtex-4 FPGA | 2007 |

## B.    Anticipation

Google contends that the following prior art anticipates the asserted claims of the patents-in-suit under 35 U.S.C. § 102:

- Belanović / Belanović and Leeser

- GRAPE-3

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here, too, Singular's Infringement Contentions appear to render this language at least ambiguous

(if not entirely meaningless) by conflating "inputs" with "numerical values." These and

potentially other indefiniteness issues may be the subject of claim construction briefing and

argument.

Respectfully submitted,

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